CUSTOMER NO.: 24498
Serial No. 10/583,822
Office Action dated: 27/10/09
Response dated: 29/03/2010

PATENT
PD030129

Remarks/Arguments

Claims 17, 18, 20, 22-24 and 26-29 are pending in the Application. Claims 17, 18, 20, 22-24 and 26-29 are rejected by Examiner. Claims 17, 23 and 27 are amended by Applicant. Claims 30-32 are added. Claims 22 and 29 are cancelled in this amendment without disclaimer or prejudice.

Amendments to the Claims

Claim 17 has been amended to more clearly recite a circuit, in which a common control signal line is connected to the control electrodes of the current control means of a multiplicity of elements via a series connection of two switching means in such a way that a corresponding multiplicity of current mirror circuits connected in parallel are at least temporarily formed when the series connection of the two switching means of the multiplicity of elements is conducting, and in which the two switching means are opened or closed responsive to respective first and second logical switching signals, which first and second logical switching signals are connected to a multiplicity of elements in a line or a column, respectively. This amendment is fully supported in the original application as will be discussed in the following.

It is clear to the person of ordinary skill in the art that the first and second switching signals must be logical signals, at least with reference to the drawings, in which the switching means are simple circuit breakers. Also, throughout the whole specification the first and second switches are either opened or closed. There is hence no room for interpreting the first and second switching signals other than logical or digital signals.

The feature of the multiplicity of current mirrors formed at least temporarily has been added in order to improve upon the clarity of the claim. It is clear from the description and the drawings that a current mirror is only present whenever the respective first and second switches of an element are closed. Whenever one of the switches of an element is opened the current mirror is no longer effective. Since it is clear that, due to possibly different image content for various pixels, the switches are not opened or closed

simultaneously, multiple current mirrors may not always be coupled in parallel, but are at least temporarily coupled in parallel.

The newly added feature of the first logical switching signal being connected to a multiplicity of elements in a line is taken from original claim 22, which is cancelled accordingly. The newly added feature of the second logical switching signal being connected to a multiplicity of elements in a column can be directly and unambiguously derived at least from figure 15 and the description thereof beginning in line 32 on page 20 and extending to line 4 on page 21 of the original application.

Claims 22 and 29 have been cancelled.

Claim 23 has been amended to provide consistent wording with and to include the limitation of amended claim 17. It is clear from the specification and the figures that the elements controlled by the first and second control signals form first and second multiplicities that have at least one element in common: the at least one common element is located at the intersection of a line and a column.

Claim 27 has been amended, corresponding to amended claim 17.

Method claim 28 corresponds to apparatus claim 20 and refers to method claim 27.

New claim 30 recites an analogue-to-digital converter that is provided for sampling the magnitude of a control signal applied to the second current control means as well as a control circuit that is adapted to generate the the logical switching signals for the first and second switching means in response to the sampled instantaneous value. New claim 30 is fully supported in the original application documents in lines 11-35 of page 16.

New claim 31 recites compensating different sensitivities of light emitting means for different colors. For compensating, the first current control means produce a current that is weighted in accordance with the different sensitivities and with respect to the reference current applied to the second current control means. New claim 31 is fully and directly supported in the original application in lines 15-28 on page 19 and the description of figure 4 beginning in line 23 on page and extending to line 8 on page 4.

New claim 32 is a method claim corresponding to claim 30.

No new matter has been added.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims17, 18, 20, 22-24, 26-29

Claims 17, 18, 20, 22-24, 26-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6.917,350 to Pae et al. ("Pae") in view of U.S Patent No. 7,138,967 to Kimura ("Kimura"). Applicant respectfully traverses the rejection.

The rejection of claims 22 and 29 has been effectively overcome by cancelling the respective claims.

As to the remaining claims, Applicant maintains the arguments defending non-obviousness provided in the response filed on October 8, 2009. In the following, additional arguments showing the non-obviousness are provided.

In the following, the term "pixel cell" is used as a synonym for the term "element" as used in the claims of the present application.

The present application involves selectively coupling one half of a current mirror to one or a group of pixel cells, each one comprising only the other half of the current mirror circuit. Thus, when the two serially connected switches of a pixel cell of the inventive circuit are closed, the half-circuit of a current mirror of the respective pixel cell is operatively connected to the other half-circuit external to the pixel cell. The reference current ramp flowing through the external half of the so-established current mirror is copied into each one of those connected pixel cells both switches of which are closed. This in turn only requires determining, or measuring, the reference current in a single point in the circuit, while still being able to know the current actually flowing in each one of the connected pixel cells. The single point in the circuit in which the reference current is determined, or measured, advantageously lies in the one half of the current mirror circuit that is shared amongst a number of complementing halves of the current mirror circuit. The inventive circuit thus substantially reduces the circuit complexity, notably with regard to the measurement circuit required for determining the current flowing in each element, or pixel cell. The inventive circuit uses the finding that the current copied in a current mirror circuit closely tracks the injected reference current. When the actual reference current reaches a level that equals the desired level for one of the pixel cells that is operatively connected in a current mirror circuit it is sufficient to open one of the two switches for that particular pixel cell. The two switches are controlled by respective logical switching signals, which are connected to a multiplicity of elements in lines or columns, respectively, allowing individual control of each element. It is noted that the current in the reference branch of the current mirror may be copied in the other branch in accordance with a factor that may be set by the design of the individual current mirrors (see e.g. figure 4 and the description thereof). However, this will still result in a linear relationship between reference current and copied current, which can easily be taken into account for determining the logical switching signals. Copied currents that have a determined ratio with respect to the reference current may be used in advantageous developments of the circuit. Applicant maintains that the concept and features of the invention as claimed in

claim 17 are not disclosed, taught or suggested in either Pae or Kimura, or the combination thereof.

The advantages of the circuit and method claimed in the present application, as set forth previously in Applicant's response filed on October 8, 2009, are they allow for programming a multiplicity of pixel cells *simultaneously* using only one single current ramp signal, and one single current measuring means provided in the driving circuit. This is an advantage because using current mirrors, or current sources in general, involves comparatively large impedances at the source side of the circuit, which may lead to slow programming due to resistances and parasitic capacitances in the circuit. If individual pixel cells were to be programmed one after the other, the slow programming may limit the refresh rate of the display. Slow programming in the current programming mode may be compensated for by providing a number of parallel circuits for programming cells in parallel, but this would undesirably increase the circuit complexity. As will be shown in the following, this and other problems are not even remotely addressed by Pae or Kimura, and as such there is no disclosure, teaching or suggestion in either of Pae or Kimura to use a circuit and a method as claimed in the present invention.

Pae discloses a driving circuit of an active matrix display device. The driving circuit includes a switching unit selectively switching a current supplied from a driving unit to the light emitting device or to a deviation compensator. The deviation compensator detects the magnitude of the current supplied from the driving unit and controls a control voltage that is applied to the driving unit in response to a reference voltage, thereby compensating luminance deviation of the display device according to threshold voltage deviation of the driving unit (see abstract). The compensation disclosed in Pae is effected by routing a current that is controlled by a current control means (P0 in Figure 2) via a switch (P3 in Figure 2) to a compensating unit (circuit shown in Figure 3). The compensation unit includes a current-to-voltage converter 21. The current from the current control means is converted into a voltage and is fed to a

comparator, where it is compared to a reference voltage that is also fed to the comparator. The output of the comparator controls a sample and hold circuit. A ramp-shaped voltage signal is supplied to the input of the sample and hold circuit. The output of the sample and hold circuit is fed to the control electrode of the current control means. When the voltage that corresponds to the current through the current control means exceeds a threshold set by the reference voltage that is fed to the comparator, the output of the comparator triggers the sample and hold circuit such that the momentary voltage of the ramp-shaped voltage signal is maintained. The driving process described above is performed during a period T4, after which the current provided by the current control means is routed to a light emitting means (OEL in Figure 2). The alternate routing of the current through the current control means to either the light emitting means or the deviation compensator can clearly be seen in the signal waveforms of Figure 4. There, the selection signal SEL and the inverted selection signal /SEL are shown, which, in Figure 2 control switches P2 and P3 in such a way that one of them exclusively conducts, while the other is opened.

According to Examiner, Pae's Vramp corresponds to the control signal line that, as claimed in claim 17 of the present application, is connected to a multiplicity of first and second switches provided with each of a respective multiplicity of elements. Examiner asserts that connection of Vramp in this way is disclosed implicitly in Pae, and also common knowledge at the time of the invention.

Examiner identifies switch P1 shown in figure 2 of Pae as corresponding to the second switching means of the circuit claimed in the present application.

Examiner then identifies the S&H circuit shown in figure 3 of Pae as corresponding to the first switching means of the invention and states that each of the circuits shown in figure 2 of Pae must include the circuit of figure 3 of Pae, because otherwise the display of Pae does not really work.

Even assuming arguendo that Vramp corresponds to the control signal line and is applied to a multiplicity of elements in parallel, and that switch P1 of Pae corresponds to the second switching means of amended claim 17, Applicant respectfully disagrees with Examiner in his assertion of the S&H circuit corresponding to the first switching means. As is clearly shown in figure 4 of Pae, the S&H circuit ***maintains*** a momentary voltage level (Vset, corresponding to Vref) when the comparator triggers, while Vramp continues to decay. A person of ordinary skill in the art would always interpret a switching means in the sense of a switch that selectively opens or closes a circuit. This is also true when referring to the drawings and the specification of the present application; all of the switching means are simple circuit breakers. Equating a circuit breaker that opens a circuit with an S&H circuit that ***maintains*** a signal is improper. Consequently, the S&H circuit of Pae cannot correspond to the first switching means of the circuit claimed in the present application.

However, for the sake of proper argumentation, in the following it is assumed that the S&H circuit of Pae corresponds to the first switching means. As will be shown in the following discussion, further differences remain between the prior art and claim 17, which render claim 17 novel and are likewise not obvious over any of the prior art references taken alone or in combination.

Examiner states that it would have been obvious to improve the circuit of Pae by repeating the S&H circuit shown in figure 3 of Pae (which Examiner identified as corresponding to the first switching means).

Applicant has combined the circuits of figures 2 and 3 as deemed obvious by Examiner. The result is shown in the drawing below (note: the circuits are taken from figures 2 and 3 of Pae, lines connecting signals "Iout" and "ramp" of figures 2 and 3 have been added).

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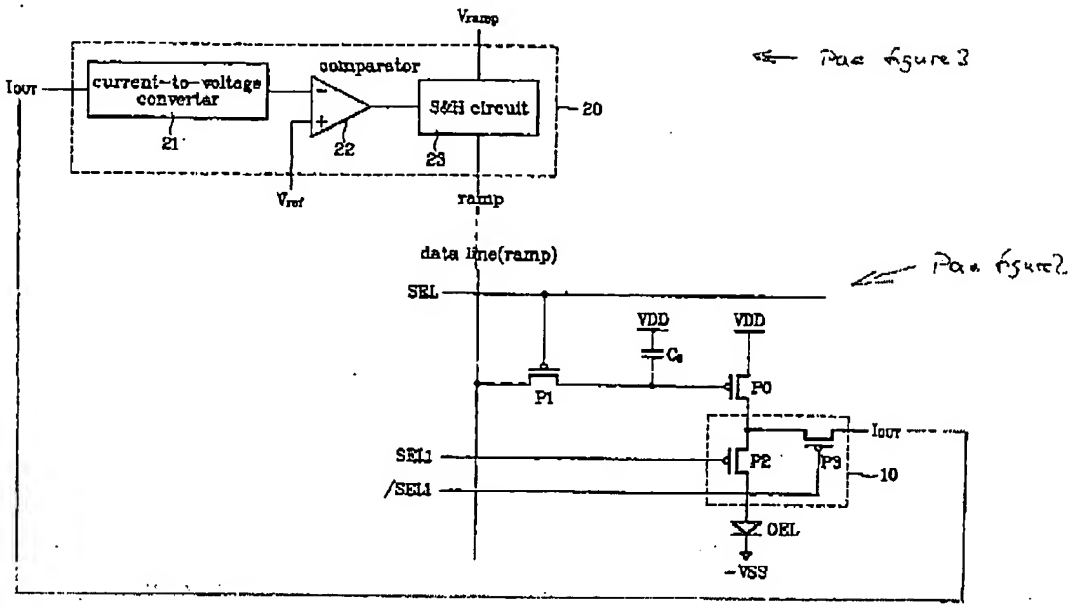

As discussed above, according to Examiner, it would be obvious to apply the signal Vramp to a multiplicity of pixel cells. (Note: this modification to Pae's circuit is not shown in the figure above.)

Examiner concludes that Pae fails to disclose a second current control means, the control electrode of which providing the signal that is applied to a multiplicity of first current control means via the control signal line in such a way that a multiplicity of parallel current mirror is present when the first and second switching means are conducting.

However, according to Examiner, the elements missing in Pae are disclosed in Kimura, enabling the person of ordinary skill in the art to make the invention. Applicant respectfully disagrees.

Figure 44 of Kimura discloses a current mirror circuit, in which the connection between the gate electrodes of the two current mirror transistors (112, 1445) can be interrupted by a series connection of two switches (1444, 1448).

Kimura teaches, in Figure 44, a current supply circuit *placed in each pixel* (emphasis added; see col. 59, lines 19 and 20). Comparing figures 44 of Kimura and Figure 7 of the present application, the current supply of Kimura comprises a current supply transistor 112 that Examiner considers corresponding to the first current control means 4. Further, Examiner considers dot sequential transistor 1448 and current holding transistor 1444 of Kimura corresponding to first and second switching means 10, 12 that are connected in series between in the feed to a control electrode of the first current control means 4. Current transistor 1445 of Kimura is considered corresponding to the second current control means 2. Current line CL of Kimura is considered corresponding to line 'i_{ramp}'. The current supply circuit of Kimura forms a current mirror circuit.

In other words, Examiner states that it would be obvious to improve the circuit of Pae by replacing the controllable voltage source (Vramp) disclosed by Pae with the current mirror as disclosed by Kimura, notably splitting the current mirror of Kimura into two halves and connecting a first half of the current mirror to a multiplicity of second halves via the first and second switching means. The added half of the current mirror corresponds to the reference branch of the current mirror, and the current flowing through it is copied in the corresponding other half in the pixel cells. In order to be functional, adding one half of a current mirror to Pae requires injecting a current ramp into the reference branch. (Note: this further modification is likewise not shown in the drawing above)

Applicant respectfully disagrees and maintains, as was explained in the response to the previous office action filed October 8, 2009, that the person of ordinary skill in the art identifies two modes for controlling an active matrix LED display,

voltage control and current control. The control methods are quite different from each other. The voltage driving mode requires a dedicated feedback loop for each element that is driven for proper uniformity of illumination, because the current control transistors in the respective light emitting elements may have different characteristics as to gate voltage vs. drain current. In contrast to that, the so-called current control mode uses the finding that the current copied in a current mirror circuit closely tracks the reference current, and that the magnitude of the current determines the light output of an LED or OLED. Thus, determining the reference current injected into the reference side of a current mirror circuit is sufficient for securely knowing the current in the mirrored side of that current mirror circuit and hence for controlling the light output of the display. Current mode control, however, requires injecting relatively small currents into the current control means, which, even when using individual current mirrors, is notorious for rather slow programming.

However, assuming arguendo that the skilled person had combined the circuits of Pae and Kimura, the resulting circuit still fails to show each and every feature of amended claim 17.

Amended claim 17 requires that the first and second switching signals are logical switching signals and are connected to a multiplicity of elements in a line or a column, respectively. Examiner identified the output signal of comparator 22 as corresponding to the first switching signal. While Kimura or Pae may disclose controlling multiple second switches P1 in one scan line by a single logical or digital second switching signal SEL, the output signal of comparator 22 is only connected within a single pixel cell, i.e. within a single element, and is a signal entirely ***internal*** to each element. Consequently, Pae fails to disclose, teach or suggest a second ***logical*** switching signal, controlling the second switching means, which is connected to a multiplicity of elements in a line.

The only further ***external*** signal disclosed in Pae that may be used for controlling the first switching means is Vref. The figure above showing the combination of Pae's figures 2 and 3 clearly shows that the desired current level to be set in the current control means P0 of each pixel cell is set by Vref. It is obvious that Vref cannot be a logical or digital control signal. Rather, it must be an analogue signal representative of the video signal for an individual element. Vref is fed to comparator 22. Vramp is passed through S&H circuit 23, and the rising (or falling) signal Vramp causes a current in P0. This current is fed to the current-to-voltage converter and the resulting voltage is fed to comparator 22. Whenever the voltage representing the current through P0 exceeds Vref (that is set to a desired level), S&H circuit 23 ***maintains*** the present output signal corresponding to Vref. Consequently, Pae fails to disclose, teach or suggest a second switching signal, controlling the second switching means, which is a ***logical*** switching signal, and which is ***connected to a multiplicity of elements in a line or column***, respectively.

It is apparent to one skilled in the art that connecting the output signal of comparator 22 or Vref of Pae to a multiplicity of elements would result in all elements connected in such way always providing the same light output, which clearly is incompatible with purpose of the desired display, notably being able to individually control each element. Consequently, Pae cannot even be used as a starting point for improving the circuit by connecting multiple elements to the same output of comparator 22 or Vref.

For the differences in the driving modes of Pae and Kimura, the skilled person will not find the faintest motivation in either Pae of Kimura to combine the teachings of the two references, notably to replicate some components in each pixel, to replace a voltage source with a current mirror, and to distribute the components as claimed in the present patent application. Applicant submits that the partitioning of the components itself constitutes an invention on its own and is not obvious nor a matter of simple choice to the person of ordinary skill in the art. As to the partitioning of the circuitry of

the current mirrors, Applicant's amendment clearly indicates which component is repeated with each pixel cell, and which component is provided once for a multiplicity of pixel cells.

In view of the discussion above, Applicant maintains that the combination of the disclosures of Pae and Kimura fails to disclose, teach or suggest all elements of amended claim 17, notably a first logical switching signal that is connected to a multiplicity of first switching means of elements in a line or a column. Consequently, amended claim 17 is not obvious over Pae in view of Kimura and is allowable.

The same arguments as presented for claim 17 apply to claim 27. Adding the disclosure of Kimura to what is disclosed by Pae fails at least to disclose or render obvious a first logical switching signal that is connected to a multiplicity of first switching means of elements in a line or a column.

New claim 30 is clearly directed to measuring the control signal applied to the second current control means in one point, while the second current control means is connected to a multiplicity of first current control means. Neither Pae nor Kimura disclose, teach or suggest an A-to-D converter for determining the magnitude of the control signal in one single point, and using the determined magnitude for opening individual of the first or second switches of a plurality of elements, relying on the function of the current mirror and on the assumption that the current through the current control means of an element, the switch of which is to be opened, closely tracks (or corresponds) to the current injected into the current mirror.

New claim 31 is directed to compensating different sensitivities of light emitting means for different colors. For compensating, the first current control means produce a current that is weighted in accordance with the different sensitivities and with respect to the reference current applied to the second current control means.

Neither Pae nor Kimura disclose, teach or suggest such weighting of the mirrored current.

In view of the discussion above, the display of claims 17 and 27 is not obvious and is patentable over Pae in view of Kimura. Claims 18, 20 and 28-31 are properly depending from allowable claims 17 and 27, respectively. As such, Applicant respectfully request that the Examiner withdraw the rejection to claims 17, 18, 20 and 27-28 and pass the claims to issue.

Likewise, the method recited in claims 23, 24 and 26 is also not obvious over the two references, since Pae teaches a closed loop control for a voltage drive control of the display, while Kimura teaches a control of the display using a constant current that is set once and then pulse modulated. These two control methods are completely different from each other and cannot be mixed with each other in order to obtain the method presented in the present application without involving substantial inventive activity. Further, the method includes structural limitations corresponding to those of claim 17, which limitations are not disclosed, taught or suggested by either of Pae or Kimura.

New claim 32 is a method claim corresponding to new claim 30 and is likewise neither anticipated by nor obvious over Pae and Kimura.

Claims 24, 26 and 32 are allowable at least for being properly dependent from allowable claim 23.

In view of the foregoing discussion, the method of claims 23, 24, 26 and 32 is not obvious and is patentable over Pae in view of Kimura. As such, Applicant respectfully requests that the Examiner withdraw of the rejection to claims 23, 24 26 and pass the claims to issue.

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Conclusion

Applicant respectfully submits that the amended pending claims patentably distinguish over the cited art and respectfully requests reconsideration and withdrawal of the 35 U.S.C. §103 rejection of the pending claims. Renewed reconsideration for a Notice of Allowance is respectfully requested.

Please charge any fees that may be due to Deposit Account No. 07-0832.

Respectfully submitted,
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